

Pipelining (II)

Pipelining Calculation

- **Speedup** is used to measure the performance of pipelining. It's calculated as follow:

- Let τ be the maximum cycle time for a pipelining stage, and τ is defined as

$$\tau = \max_i(\tau_i) + d = \tau_m + d$$

τ_i : the logic delay for *stage_i*

τ_m : the maximum logic delay for any stage

d : latch delay

- The speedup is calculated as follow

$$Speedup = \frac{\text{Time to execute N instructions on the single-stage}}{\text{Time to execute N instruction on K stages}} = \frac{NT_1}{[K + (N - 1)]\tau}$$

T_1 : the single-stage logic delay plus the latch delay

Example

- Assume there is a four-stage CPU. Each stage completes one step of the four steps of instruction execution: fetch, decode, execute, and write back. The logic delay for each step is 5 ns, and the latch delay is 1 ns. Answer the following questions.

- What is the time to execute one instruction on the 4-stage CPU?

$$(5 + 1) * 4 = 24 \text{ ns}$$

- Assume there is a single-stage CPU that completes all four steps in one stage. What is the time to execute one instruction on the single-stage CPU?

$$5 * 4 + 1 = 21 \text{ ns}$$

- What is the time to execute five instructions on the single-stage CPU?

$$5 * 21 = 105 \text{ ns}$$

- What is the time to execute five instructions on the four-stage CPU?

$$(4 + 5 - 1) * (5 + 1) = 48 \text{ ns}$$

- What is the speedup for 5 instructions using the four-stage CPU?

$$105/48 = 2.2$$